IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

JUSTIN K. BRASK
MARK L. DOCZY
SCOTT A. HARELAND
JOHN P. BARNAK
MATTHEW V. METZ
JACK KAVALIEROS
ROBERT S. CHAU

Serial No.: 10/652,796

Filed: August 28, 2003

For: A METHOD FOR MAKING A SEMICONDUCTOR DEVICE HAVING A HIGH-K GATE DIELECTRIC

Art Unit: unknown

Examiner: unknown

Attorney Docket: P17280

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

This Information Disclosure Statement is being submitted under 37 C.F.R. §1.97(b). Enclosed is a copy of Information Disclosure Citation Form PTO-1449 together with copies of the references cited on that form. It is respectfully requested that the cited references be considered and that the enclosed copy of Information Disclosure Citation Form PTO-1449 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

Pursuant to 37 C.F.R. § 1.97, the submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made

and is not to be construed as an admission that the information cited in this statement constitutes prior art or is otherwise material to patentability.

Respectfully submitted,

Dated: October 30, 2003

Mark V. Seeley
Reg. No. 32,299

Intel Corporation
Mail Stop SC4-202
2200 Mission College Blvd.
Santa Clara, CA 95052-8119
(408) 765-7382

FIRST CLASS CERTIFICATE OF MAILING
(37 C.F.R. § 1.8(a))

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class mail with sufficient postage in an envelop addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on

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Mark Seeley
Name of Person Mailing Correspondence

Signature

October 30, 2003
Date

LJV/cak (10/01/97)

Form PTO-1449 (Modified)	Atty Docket No.: P-3880	Serial No.: 10/652,796
List of Patents and Publications Statement (Use several sheets if necessary)	NOV 0 6 2003 PATENT & TRADEMARK OFFICE TC 2826	**Applicant:** Justin K. Brask et al. **Filing Date:** August 28, 2003

REFERENCE DESIGNATION		U.S. PATENT DOCUMENTS				
Examiner Initials		Document No.		Class	Sub-Class	Filing date if appropriate
	AA	6,121,094	Gardner et al.	438	287	
	AB	6,436,777	Ota	438	305	
	AC	6,514,828	Ahn et al.	438	297	
	AD	6,617,209	Chau et al.	438	240	
	AE	6,617,210	Chau et al.	438	240	
	AF	US2002/0197790	Kizilyalli et al.	438	240	
	AG	US2003/0045080	Visokay et al.	438	591	
	AH					
	AI					
	AJ					
	AK					
	AL					
	AM					
	AN					
	AO					
	AP					

FOREIGN PATENT DOCUMENTS

No.		Document No.	Date	Country	Class	Sub-Class	Translation
	AQ						
	AR						
	AS						
	AT						
	AU						

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

	AV	Polishchuk et al., "Dual Workfunction CMOS Gate Technology Based on Metal Interdiffusion," www.eesc.berkeley.edu, 1 page.
	AW	
	AX	
	AY	
	AZ	

Examiner	Date Considered

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.